IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kuzmenka	Docket No.:	2002 P 11260 US
Serial No.:	10/715,145	Art Unit:	2181
Filed:	November 17, 2003	Examiner:	TBD
For:	Memory System and Memory Subsystem		

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Transmittal of Certified Copy of Priority Document

Dear Sir:

Attached please find a certified copy of the foreign application from which priority is claimed for this case:

Country:	Europe
Application Number:	02026015.4
Filing Date:	November 21, 2002

Respectfully submitted,

Ira S. Matsil
Reg. No. 35,272
Attorney for Applicant

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, TX 75252
Tel: 972-732-1001
Fax: 972-732-9218

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Bescheinigung | Certificate | Attestation

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02026015.4

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 02026015.4
Demande no:

Anmeldetag:
Date of filing: 21.11.02
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Infineon Technologies AG
St.-Martin-Strasse 53
81669 München
ALLEMAGNE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Memory system and memory subsystem

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G11C/

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR

SCHOPPE, ZIMMERMANN, STÖCKELER & ZINKLER

PATENTANWÄLTE
European Patent Attorneys
European Trademark Attorneys

Fritz Schoppe, Dipl.-Ing.
Tankred Zimmermann, Dipl.-Ing.
Ferdinand Stöckeler, Dipl.-Ing.
Franz Zinkler, Dipl.-Ing.

Telefon/Telephone 089/790445-0
Telefax/Facsimile 089/790 22 15
Telefax/Facsimile 089/74996977
e-mail: szsz_iplaw@t-online.de

Patentanwälte · Postfach 710867 · 81458 München

Infineon Technologies AG
St.-Martin-Str. 53

81669 München

MEMORY SYSTEM AND MEMORY SUBSYSTEM

Description

Memory system and memory subsystem

The present invention relates to a memory system, and, in particular, to a memory system having an improved data bus topology and/or control signal topology. Moreover, the present invention relates to a memory subsystem for such a memory system.

One conventional memory system which is implemented nowadays in a wide spread manner is the DDR1 memory subsystem.

In a DDR1 memory subsystem, a memory controller and a number of slots are arranged on a memory board. The slots are for receiving connectors of DDR DRAM modules. The DDR DRAM modules include a module board and respective memory chips arranged on the module board. Signal buses are provided for transferring signals between the memory chips and the controller, i.e. for transferring clock signals, data signals and control signals therebetween. The control signals are typically C/A signals (C/A = command/address).

In the following, bus topologies of the DDR1 memory subsystem and of the successor thereof, i.e. the DDR2 memory subsystem, are set out making reference to Fig. 11 to 13a.

Fig. 11 schematically shows the data bus topology of the DDR1/DDR2 memory subsystem. A memory controller 10 is arranged on a circuit board (not shown) of the memory subsystem. A data bus 12 is arranged on the circuit board and connected to the controller 10. In addition, the data bus 12 is connected to slot connectors 13 having respective slots for receiving DDR1/DDR2 memory modules 14. On the modules 14, i.e. the module board thereof, respective data lines 16 are arranged which connect DDR DRAM chips 18 arranged on the module boards to the data bus 12. Moreover, the data bus 12 is connected to a ref-

erence potential via a termination resistor 20 at the end opposite to the memory controller 10.

Thus, in existing DDR1/DDR2 memory subsystems, the data bus topology includes a linear data bus 12 on the circuit board (or motherboard) of the memory system and stub buses 16 to the memory chips 18 arranged on the memory modules 14.

A unbuffered clock topology for DDR1/DDR2 memory systems is shown in Fig. 12a. For sake of simplicity, differential traces are shown like single ended once in Fig. 12a. As can be seen in Fig. 12a, the controller 10 is connected to a phase locked loop 22 (PLL) via a clock line 24. The phase locked loop 22 generates clock signals on a plurality of twelve clock sublines 26. Respectively, three clock sublines 26 are connected to each of the memory modules 14, which are received in slots 1 to 4 as it is indicated in Fig. 12a. In Fig. 12a, the memory module inserted into slot 1 is shown as having nine DDR DRAM chips 18. The memory modules inserted in slots 2 to 4 are not drawn to this detail. Moreover, each clock subline 26 branches into three clock sub-sublines 28 each of which is connected to a respective memory chip 18. PLL feedback traces are not shown in the figures. Although four modules for the unbuffered clock topology are shown in Fig. 9a, usually no more than three modules are used in PC desktop systems.

In the clock bus topology shown in Fig. 12a, one part of the clock sublines 26 is formed on the memory board and one part thereof is formed on the module board. Both parts are connected via the slot connector into which the memory module is inserted. The clock sub-sublines 28 are formed on the memory boards. In the unbuffered clock topology shown in Fig. 12a, clock signals must be simultaneously delivered to all DRAM chips.

A registered clock topology for DDR1/DDR2 memory systems is shown in Fig. 12b.

In this topology, a phase locked loop 30 is provided on the respective memory modules 14. The memory controller 10 is connected to the phase locked loops 30 of the memory modules 14 by a respective clock line 32. The phase locked loop 30 comprises a number of output lines 34 corresponding to the number of memory chips 18. In the clock topology shown in Fig. 12b, runtime differences due to different lengths of the clock lines 32 can be equalized by the phase locked loops 30.

An unbuffered bus topology for C/A buses of the DDR1/DDR2 memory system is shown in Fig. 13a, whereas a registered bus topology for the C/A buses of a DDR1/DDR2 memory system is shown in Fig. 13b.

In the unbuffered C/A bus topology, a C/A bus 40 is provided on the memory circuit board and connected to a reference potential by a termination resistor 42. A common C/A bus portion 44 of the respective memory modules 14 is connected to the C/A bus 40 via respective slot connectors 45. The common C/A bus portion 44 branches in C/A subbuses 46 each of which is connected to a respective DDR DRAM chip 18. In Fig. 13a, only one address line of the C/A bus topology is shown, whereas, in reality, a plurality of 21 to 27 address lines may be provided.

In the registered C/A bus topology shown in Fig. 13b, each of the memory modules 14 comprises a register 50 which is connected to a C/A bus 52 on the memory circuit board via the slot connectors 45. Again, the C/A bus 52 is connected to a reference potential via a termination resistor 54 at the end opposite to the memory controller 10.

The inventors have recognized that the signal quality in a DDR2 system having four slots and operating at a data rate of 533 Mb/s is not acceptable in case of using a data bus topology like in a DDR1 memory subsystem shown above making reference to Fig. 11.

It is the object of the present invention to provide a memory system permitting an improved signal quality at high data rates and to provide a memory subsystem and a memory module which can be used in such a memory system.

This object is achieved by a memory system according to claim 1 and a memory subsystem according to claim 11.

The present invention provides a memory system comprising:

a circuit board having a first means for receiving and a second means for receiving;

a first memory module received in the first means for receiving;

a second memory module received in the second means for receiving; and

a flexible bridge connecting the first and second memory modules for providing a signal bus between the memory modules.

The present invention further provides a memory subsystem comprising:

a first memory module, a second memory module, and a flexible bridge connecting the first and the second memory modules and providing a signal path therebetween.

The present invention is based on the recognition that the usage of a flexible bridge for a signal bus between two modules allows to connect all memory modules, and, thus, all memory chips on the memory modules, without stubs, and, therefore, to make signal quality better. Such a stub-less topology can be referred to as SLT topology (SLT = short loop through) in view of the fact that all memory modules are connecte in one loop.

Thus, in preferred embodiments of the present invention, the signal bus between the memory modules which is implemented as a flexible bridge is a data bus so that the quality of the signals transferred over the data bus can be improved.

In preferred embodiments of the present invention, the first and second means for receiving are slot connectors provided on the circuit board of the memory system and the memory modules comprise memory module boards inserted into the slot connectors so that the memory module boards are oriented substantially perpendicular to the memory system circuit board and so that electrical connections are achieved between respective signal lines on the memory system circuit board and the memory module board. In such case, the flexible bridge, in the form of a flexible PCB (PCB = printed circuit board), for example, is connected at the end of the memory module board opposite to the end inserted into the slot connector. Signal lines on the flexible bridge are connected to respective signal lines on the memory module board, so that a signal bus connecting the memory modules is obtained. Preferably, the signal bus includes a data bus, but also may include a control signal bus and/or a clock bus. To be more specific, in a preferred embodiment of the present invention, the data bus between specific memory modules is implemented via the flexible bridge whereas the clock bus topology and the control signal bus topology correspond to the conventional DDR1/DDR2 memory system topologies.

If, in a four slot system, memory modules are inserted into each slot, according to the present invention, a data bus between a memory controller and a first memory module is routed over the memory system circuit board, a data bus between the first memory module and a second adjacent memory module is implemented via a flexible bridge, a data bus between the second memory module and a third memory module is routed over the memory system circuit board, a data bus between the third memory module and an adjacent fourth memory module is implemented via a flexible bridge, and a data bus between the fourth mem-

ory module and a termination resistor located on the memory system circuit board is routed over the memory system circuit board. By this arrangement, all memory chips on the memory modules can be connected by the data bus without stubs.

In case a four slot memory system is populated by two memory modules only, the first module is to be inserted into the first slot while the second module is to be inserted into the fourth slot. Then, the data bus between the first and second modules can be implemented making use of a flexible bridge so that a continuous data bus between the memory controller and the termination resistor is realized.

Making use of the present invention in a memory system having dimensions comparable to those of DDR2 4 slot memory system, a good signal quality at 533 Mb/s can be achieved, while the conventional topology shown in Fig. 11 does not show an acceptable performance at such a data rate. In the present invention, conventional DDR2 chips can be used without changes being necessary thereto. Moreover, it is possible to use the standard for the connector pinout of 2 slot systems and DIMM dimensions (DIMM = dual inline memory module). The present invention is not restricted to a 4 slot topology indicated above. Rather, the number of slots can be increased to six or higher, and correspondingly the number of "pairs" of memory modules connected via the flexible bridge can be increased to three or higher, so that high density systems can be obtained. According to the invention, it is possible to use existing 240 pin slot connectors. Moreover, the present invention renders superfluous usage of any stub resistors on the data bus.

Preferred embodiments of the present invention are described hereinafter making reference to the enclosed drawings, in which:

Fig. 1 shows a schematic side view of an embodiment of an inventive memory system;

Fig. 2 shows a schematic side view of a further embodiment of an inventive memory system;

Fig. 3shows a schematic view of a data bus topology achievable by the present invention;

Fig. 4 shows a schematic view of C/A bus topology achievable by the present invention;

Fig. 5 a shows a diagram for further explaining the embodiment shown in Fig. 1;

Fig. 6 and 7 show representations of data signals obtained from the system shown in Fig. 5;

Fig. 8 an alternative embodiment of an inventive memory system;

Fig. 9 a modification of the embodiment of the invention shown in Fig. 1;

Fig. 10 a memory system providing a reduced capacity;

Fig. 11 shows an existing data bus topology;

Fig. 12a and 12b show existing clock bus topologies; and

Fig. 13a and 13b show existing C/A bus topologies.

The embodiment of a memory system according to the invention shown in Fig. 1 comprises a memory circuit board 100 which is named motherboard in the following. A memory controller 102, a first slot connector 104, a second slot connector 106, a third slot connector 108, a fourth slot connector 110 and a termination resistor 112 are arranged on the motherboard 100. First, second, third and fourth memory modules 114, 116, 118 and 120 are inserted into the first to fourth slot connectors 104, 106, 108 and 110. Each of the memory modules includes a number

of memory chips 130 arranged on a respective memory module board 132.

As can be seen in Fig. 1, a flexible bridge 138 is provided between the first and second memory modules 114, 116, and a flexible bridge 140 is provided between the third and fourth memory modules 118, 120. The flexible bridge is preferably formed by a flexible printed circuit board having two conductive layers, a reference potential layer and a signal layer, and at least one isolating layer isolating the conductive layers from each other. The isolating layer may be formed of any suitable material providing the desired flexibility, a polymer material, for example. In addition, the flexible bridge may be provided with further isolating layers and protective layers.

In the following, the data path and, therefore, the data bus of the memory system shown in Fig. 1 is explained in detail.

A first portion of the data path is provided by a data bus portion 150 provided on the motherboard 100 between the memory controller 102 and the first slot connector 104. A second portion of the data path is provided by data lines 152 formed on the memory module board 132 of the first memory module 114. The memory chips of this memory module also are connected to the data lines 152. The data lines 152 on the memory module board are connected to the first data bus portion 150 by electrical connectors 154 of the slot connector 104, wherein the slot connector and the electrical connectors can be of a conventional construction.

The data lines 152 on the memory module board 132 extend from the lower end thereof (at which they are connected by the electrical connectors 154 to the data bus portion 150) to the upper end of the memory module board at which same are connected to respective data lines on the flexible bridge 138 so that the flexible bridge 138 forms a third data bus portion. A fourth data bus portion 156 is formed by data lines on the memory module board of the second memory module 116, and a

fifth data bus portion 158 is formed by data lines located on the motherboard 100 and providing electrical connection between the slot connectors 106 and 108. A sixth data bus portion 160 is formed by data lines on the memory module board of the third memory module 118, a seventh data bus portion is formed by the flexible bridge 140, an eight data bus portion is formed by data lines on the memory module board of the fourth memory module 120, and a ninth data bus portion 164 is formed by data lines on the motherboard 100 connecting the electrical connectors 154 of the fourth slot connector 110 to a first ends of a termination resistor 170. The second end of the termination resistor 170 is connected to a reference potential plane 172 of the motherboard 100.

The flexible bridges 138 and 140 can be implemented as separate flexible printed circuit boards wherein respective pads thereof are soldered to associated pads of the memory modules, i.e. the DIMMs. Alternatively, the flexible bridges can be formed as a common part of some layers of adjacent memory modules.

In the embodiment shown in Fig. 1, a first pair of modules, DIMM 1-2, is connected via the flexible bridge 138 and a second pair of memory modules, DIMM 2-3, is connected via the flexible bridge 140. According to Fig. 1, all four slots are populated by memory modules and the memory chips of all modules can be connected by a data bus without bus stubs.

Fig. 2 shows the situation for the case that the memory system is populated by two memory modules 114 and 116 only. In this situation, the first memory module 114 is inserted into the first slot connector 104 and the second memory module 116 is inserted into the fourth slot connector 110. Again, the first and second memory modules are connected via the flexible bridge 138. Thus, for the two memory modules used, the data bus is formed by the portions 150, 152, 138, 162 and 164. Again, a continuous data bus without stub buses is achieved.

As can be derived from Fig. 1 and 2, preferably the flexible bridges 138 and 140 are designed such that the respective pair of memory modules, DIMM 1-2 or DIMM 2-3, can be used according to Fig. 1 and according to Fig. 2. To this end, the flexible bridge and, thus, the signal lines thereof, have to be provided with a sufficient length.

The arrangement of a pair of memory modules connected via the flexible bridge can be sold as a separate package.

In Fig. 1 and 2, a second row of electrical connectors 174 of the slot connectors 104, 106, 108 and 110 are connected to the reference potential plane 172, whereas the electrical connectors 154 are connected to respective data bus portions.

In the embodiments described above with respect to Fig. 1 and 2, the data bus between respective pairs of modules is implemented making use of a flexible bridge. The C/A bus topology and the clock bus topology can be realized as in existing systems. A schematic view of the data bus obtained in the embodiment of Fig. 1 is shown in Fig. 3 in which the data bus portion provided by the flexible bridges 138 and 140 are indicated as loop portions 176.

In alternative embodiments of the present invention flexible bridges between pairs of memory modules may be used for implementing C/A signal buses and/or clock buses rather than data buses or in addition to data buses.

One embodiment of a registered C/A bus topology making use of a flexible bridge 180 is schematically shown in Fig. 4. Fig. 4 shows two memory modules 200 comparable to the memory modules 14 described above with respect to Fig. 13b, i.e. comprising respective registers 50 for providing a registered C/A bus. To this end, the register 50 of the left-hand module 200 is connected to a C/A bus portion 202 formed on the motherboard (not shown) via a slot connector 45. The output of the register 50 branches into a number of C/A subbuses 204 corresponding to

the number of DDR DRAM chips 18 provided on the memory module. The C/A bus portion 206 between the memory modules shown in Fig. 4 is implemented making use of a flexible bridge 180 comprising signal lines to connect corresponding C/A bus lines on both memory modules to each other. Finally, the register 50 of the right-hand memory module shown in Fig. 4 is connected to the register of a memory module inserted into a next slot via a C/A bus portion provided on the motherboard (not shown).

Thus, a continuous C/A bus substantially without stub buses can be achieved comparable to the data bus explained above making reference to Fig. 1 and 2. In Fig. 4, for sake of simplicity, only one C/A line is shown for the C/A bus portions, while, in reality, the C/A bus portions may include a number of 21 to 27 address lines, for example.

A diagram showing a possible realization of the data bus in the embodiment shown in Fig. 1 is shown in Fig. 5. In Fig. 5 possible line lengths in mils are indicated by the numbers with which the respective line symbols are provided. 1 mil is equal to 25.4 µm, so that: 2250 mil = 57 mm; 500 mil = 12.7 mm; 50 mil = 1.27 mm; 850 mil = 21.6 mm; and 350 mil = 8.9 mm.

The trace impedance of the respective line portions is indicated in the upper left-hand corner of Fig. 5 stating that the bright line portions have a trace impedance of 60 Ohm, whereas the darker line portions have a trace impedance of 39 Ohm. It can be derived from Fig. 5 that the trace impedance is aligned along the data bus, in the embodiment shown to 39 Ohm. The short cuts of 60 Ohm traces are used for compensation of reflections. Moreover, the termination resistor 170 is shown in Fig. 5 as having a resistance of 37.5 Ohm. Moreover, according to Fig. 5, the reference potential is VDD/2, wherein VDD represents a power supply voltage.

Further shown in Fig. 5 is a controller active termination 210 comprising a resistor 222 of, for example, 37.5 Ohm connected

between the output of the memory controller 102 and a reference potential of, for example, VDD/2. The controller active termination 210 is active only during the read operation. The DRAM chips 130 send to the data bus voltage pulses which must be terminated on the ends of the bus, otherwise interpolation between reflected (from the none-terminated end) and incoming waves will distort a signal. Such reflection is prevented by the termination resistors 170 and 222. The controller active termination 210 is of a conventional structure and can be implemented by a termination resistor embedded into the chip and deactivated by a transistor switch (not shown) during write operation. In some existing products, such an active termination is also used in the DRAMs during write operation.

As can be seen in Fig. 5, a compensation capacitor 224 can be connected between the data bus portion on the motherboard and ground at the half of the length of that data bus portion, for example. The capacitance of the compensation capacitor may be 3.0 pF, for example. One of the objects of the compensation capacitor is to make the frequency characteristic of the whole system a little more linear. Moreover, EM waves reflected from this capacitor 224 compensate waves reflected from the controller 102.

In Fig. 6 and 7, data eyes for a write operation (Fig. 6) and a read operation (Fig. 7) for the system of Fig. 1 and 5 being the result of a simulation are shown. The data eyes have been obtained when making use of the following parameters.

The used data rate was 533 Mb/s and the used bit sequence was a ISI 40 bit sequence. VDD was 1.7 V. The equivalent output resistance of the memory controller 102 was 35 Ohm. The equivalent output resistance of the DRAM chips 130 was 21 Ohm. The input capacitance of the memory controller 102 was 4 pF and the input inductance thereof was 3 nH. The input capacitance of the DRAM chips was 4 pF and the inductance thereof was 3 nH. The above parameter indicating the capacitances of the controller and the chips is mainly determined by parasitic

capacitances of a pin and the capacitance connected to such a pin (caused by pin transistors on the chip and so on, for example). The inductances of the memory controller and the DRAM chips are mainly caused by the parasitic inductances of the chip packages.

The data eyes shown in Fig. 5 and 6 were obtained when making use of a resistor driver model with a resistance of the resistors 127 and 222 of 37.5 Ohm and a rise/fall time of 0.25 ns.

Open data eyes were measured at levels VDD/2 +/-250 mV, wherein these levels are shown by respective lines 230 in Fig. 6 and 7. Moreover, the duration of the respective open data eyes are indicated in Fig. 6 and 7.

The data eyes shown in Fig. 6 and 7 have been obtained by making use of a bridge length of 850 mil (about 21.6 mm) (see Fig. 5). However, further simulations showed that comparable results without any degradation of signal quality could be obtained making use of longer bridge lengths of 1200 mil (about 30.5 mm), for example.

In Fig. 8 an alternative configuration of an inventive memory system is shown, wherein the memory modules 114 and 116 are arranged parallel with respect to a motherboard 304. The memory module 114 is connected to the motherboard 304 via a first connector 306 and the memory module 116 is connected to the motherboard 304 via a second connector 308. Again, the modules 114 and 116 are connected the flexible bridge 138 to provide a continuous data bus without making use of stubs. Such a configuration is appropriate for laptops, for example. The memory subsystem comprising both memory modules and the flexible bridge shown in Fig. 8 may be identical to that described with respect to Fig. 1.

Fig. 9 shows a modification of the embodiment of the invention shown in Fig. 1. According to Fig. 9, a termination resistor 320 is arranged on a memory module 116'. Thus, the terminator

is arranged directly on the memory subsystem, i.e. the "double module" having a flexible bridge. In such a case, a termination on the motherboard is no longer necessary. Thus, it would be possible to populate two adjacent slots of a motherboard having four slots only (the motherboard of Fig. 1, for example, with or without the termination resistor 170) while still obtaining an appropriate termination of the data bus. Alternatively, the motherboard could include two slots only.

A motherboard 400 having two slots 402 and 404 of which only slot 404 is populated with a memory module 406 is shown in Fig. 10. The memory module 406 has arranged thereon a termination resistor 320 so that a complete data bus is obtained even in case only the slot 402 is populated.

Systems having only one or two memory modules may be considered for applications in which a reduced amount of memory is needed, non-server PC systems, for example.

In the above specification, the reference potential plane can be formed by a ground plane in single ended systems and can be formed by a predetermined potential of VDD/2, for example, in differential systems.

List of Reference Numbers

10	memory controller
12	data bus
13	slot connectors
14	memory modules
16	data lines
18	DDR DRAM chips
20	termination resistor
22	PLL
24	clock line
26	clock sublines
28	clock sub-sublines
30	PLL
32	clock line
34	output lines
40	C/A bus
42	termination resistor
44	common C/A bus portion
45	slot connectors
46	C/A subbuses
50	register
52	C/A bus
54	termination resistor
100	motherboard
102	memory controller
104, 106, 108, 110	slot connectors
112	termination resistor
114, 116, 118, 120	memory modules
130	memory chips
132	memory module board
138, 140	flexible bridges
150	first data bus portion
152	second data bus portion
154	electrical connectors
156	fourth data bus portion
158	fifth data bus portion
160	sixth data bus portion

162	eight data bus portion
164	ninth data bus portion
170	termination resistor
172	reference potential plane
174	electrical connectors
176	loop portions
180	flexible C/A bus bridge
200	memory module
202	C/A bus portion
204	C/A subbus
206	C/A bus portion
208	C/A bus portion
210	active termination
222	resistor
224	compensation capacitor
230	predetermined voltage levels
304	motherboard
306	first connector
308	second connector
320	termination resistor
116'	memory module
400	motherboard
402, 404	slots
406	memory module

Claims

1. A memory system comprising:

a circuit board (100; 304) having a first means (104; 306) for receiving and a second means (106; 308) for receiving;

a first memory module (114) received in said first means (104; 306) for receiving;

a second memory module (116) received in said second means (106; 308) for receiving; and

a flexible bridge (138) connecting said first and second memory modules (114, 116) for providing a signal bus between said memory modules (114, 116).

2. The memory system of claim 1, wherein the memory modules (114, 116) are received in the respective means (104, 106; 306, 308) for receiving at a first side thereof and wherein the flexible bridge (138) extends from a respective second side of the memory modules (114, 116).

3. The memory system of claim 1, wherein the respective second side of the memory module (114, 116) is arranged opposite to the first side thereof.

4. The memory system of one of claims 1 to 3, wherein the receiving means (104, 106; 306, 308) are slots for receiving memory modules adapted for DDR memory systems.

5. The memory system of one of claims 1 to 4, wherein the flexible bridge (138) comprises data lines and/or control signal lines for providing a data bus (176) and/or a control signal bus (206) between said memory modules (114, 116).

6. The memory system of one of claims 1 to 5, wherein a memory controller (102) and signal lines (150, 158, 164) are provided

on said circuit board (100), wherein said signal lines provide a data bus and/or a control signal bus between said controller (102) and said first memory module (114).

7. The memory system of claim 6, wherein said signal lines on said circuit board (100) further provide a clock bus between said memory controller (102) and said memory modules.

8. The memory system of claim 6 or 7, further comprising a third memory module (118) received in a third means (108) for receiving and wherein said signal lines on said circuit board (100) further provide a data bus and/or a control signal bus between said second and said third memory modules (116, 118).

9. The memory system of one of claims 1 to 8, wherein the bridge (138) is a flexible printed circuit board having a ground layer and a signal layer.

10. The memory system of one of claims 1 to 9, wherein said signal bus provided by said flexible bridge (138) has a trace impedance adapted to a trace impedance of buses on the memory module (114, 116) and the circuit board (100) to which said signal bus is connected.

11. A memory subsystem comprising:

a first memory module (114), a second memory module (116), and a flexible bridge (138) connecting the first and the second memory modules (114, 116) and providing a signal path therebetween.

Summary

Memory system and memory subsystem

A memory system has a circuit board (100) provided with a first slot connector (104) into which a first memory module (114) is inserted. A second slot connector (106) is provided into which a second memory module (116) is inserted. The first and the second memory modules (114, 116) are connected via a flexible bridge (138). The flexible bridge extends from respective ends of the memory modules opposite to that ends thereof which are inserted into the connector slots. The flexible bridge (138) provides a signal bus between the memory modules (114, 116).

Fig. 1

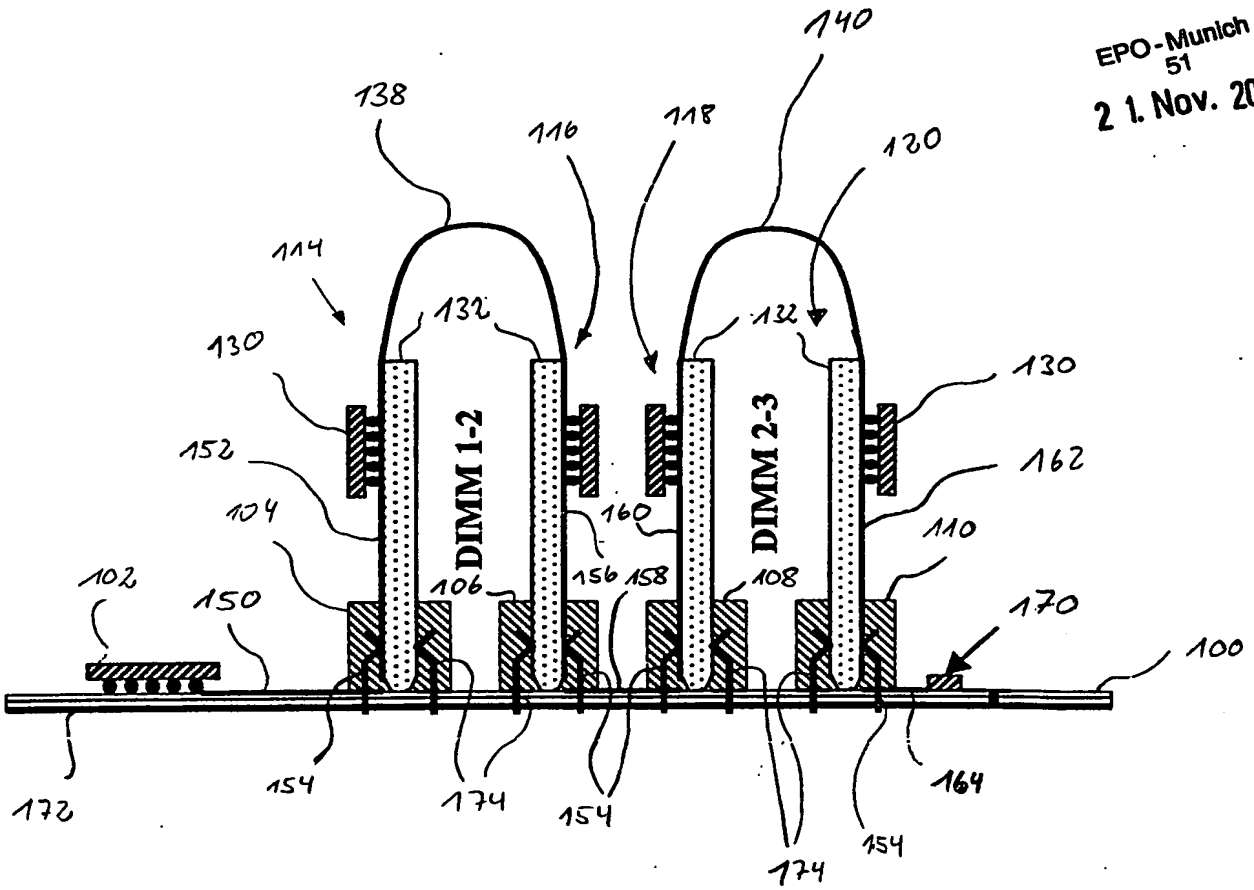

Fig. 1

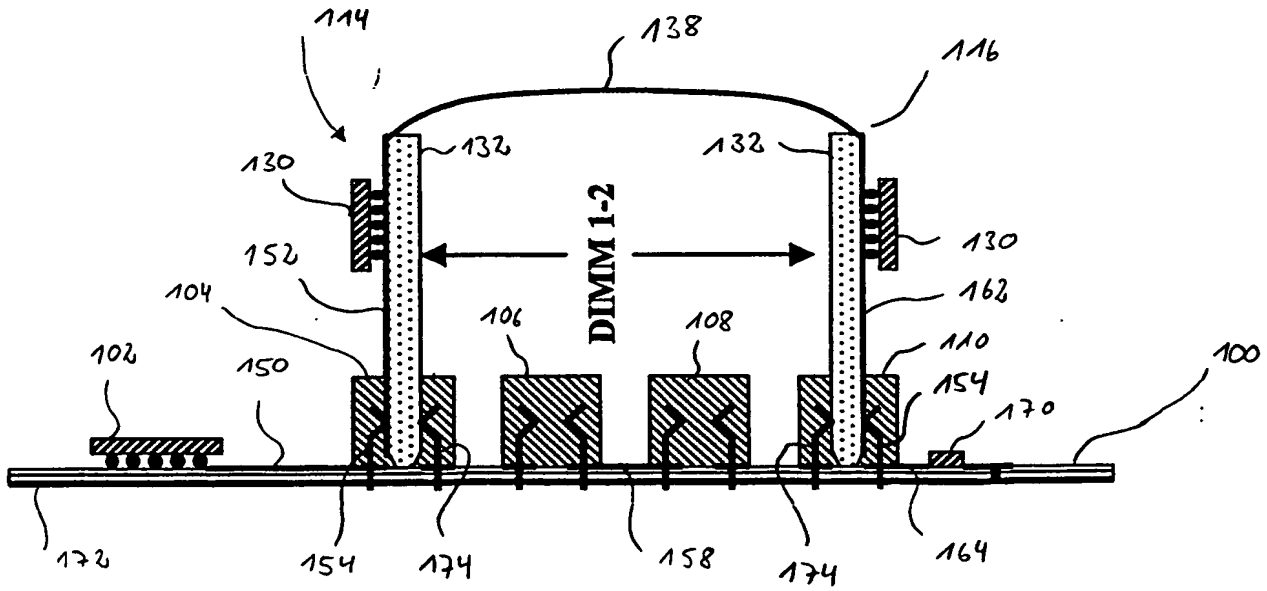

Fig. 2

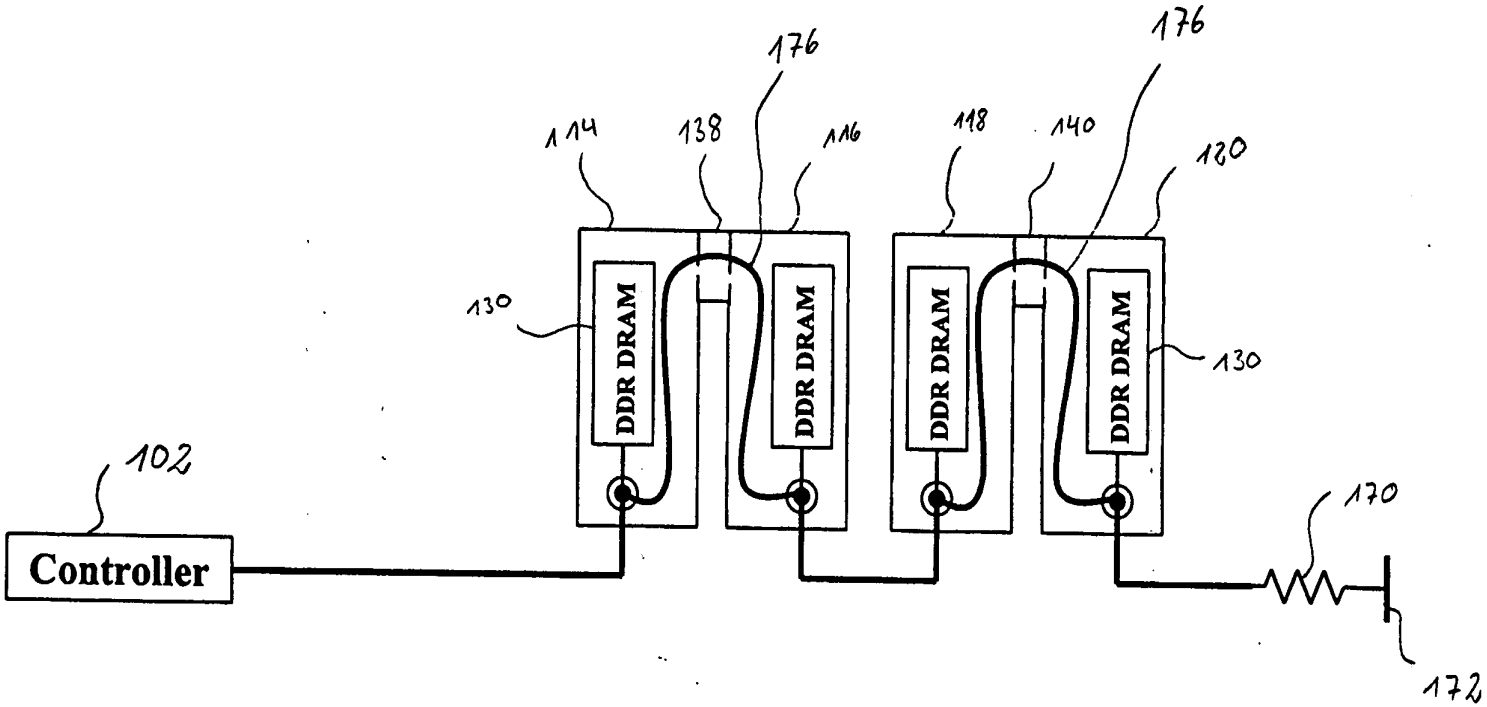
176
176
114
138
116
118
140
120
130
DDR DRAM
DDR DRAM
DDR DRAM
DDR DRAM
130
102
Controller
170
172

Fig. 3

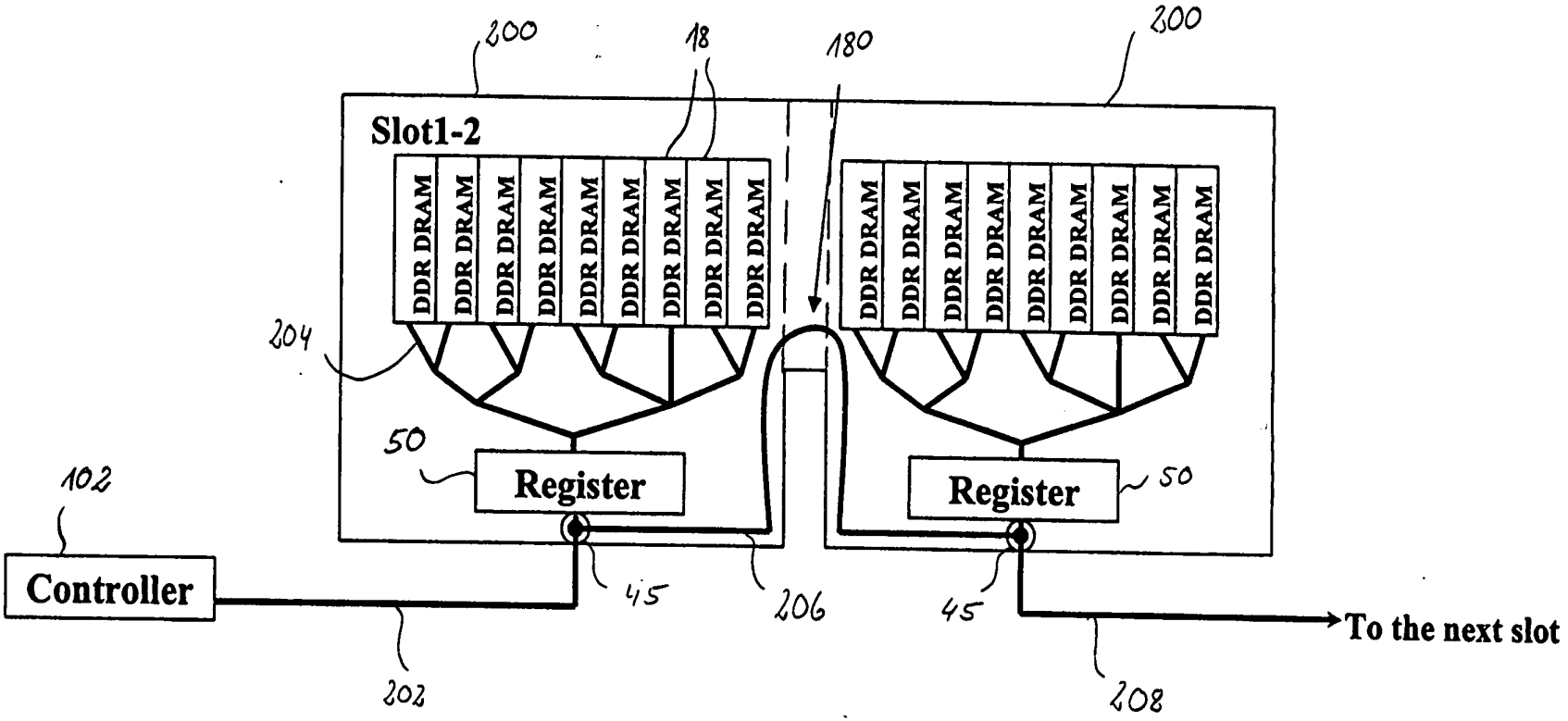
300
18
180
300
Slot1-2
DDR DRAM
204
50
Register
Register
50
102
Controller
45
206
45
To the next slot
202
208

Fig. 4

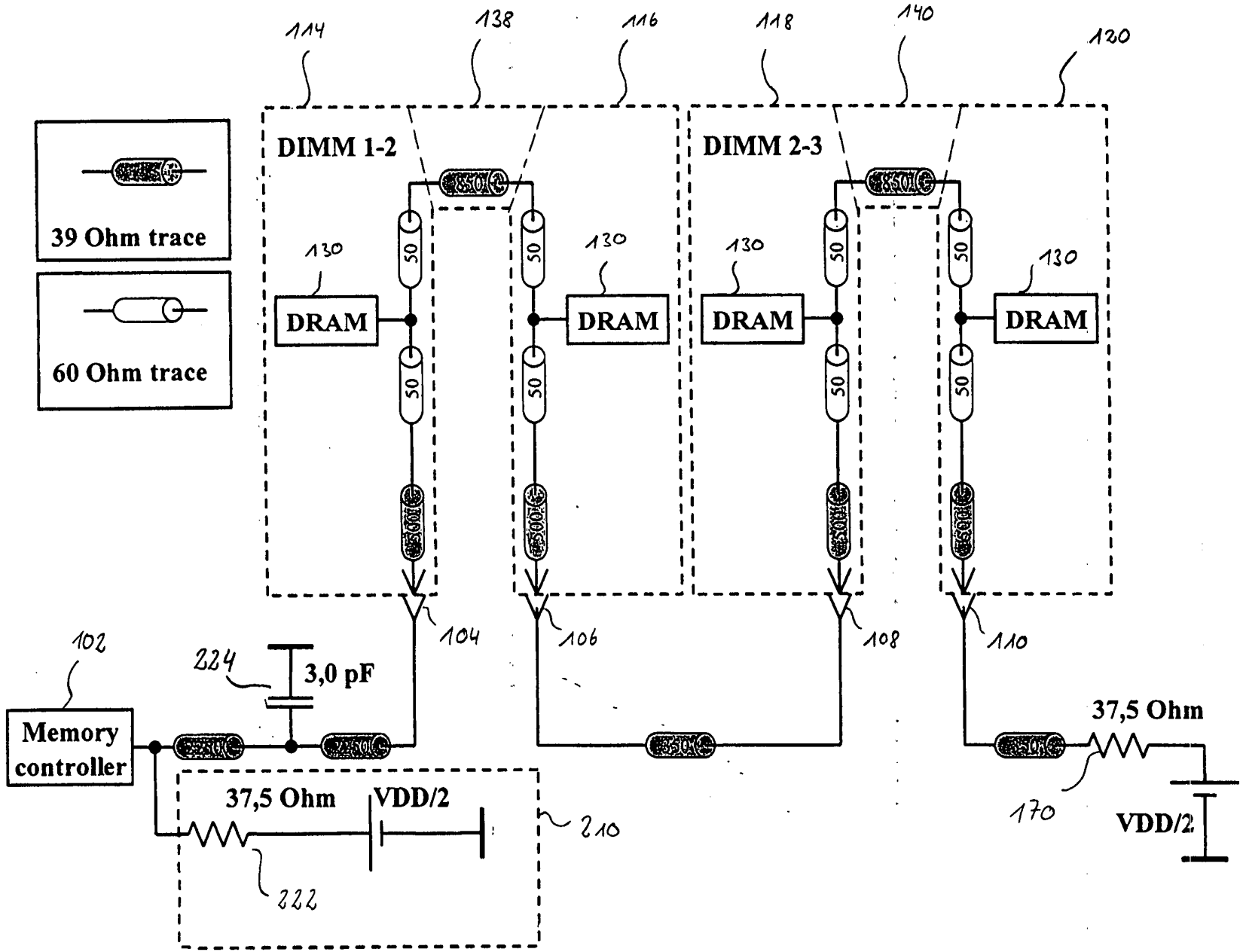
39 Ohm trace
60 Ohm trace
DIMM 1-2
DIMM 2-3
DRAM
DRAM
DRAM
DRAM
130
130
130
130
50
50
50
50
50
50
50
50
50
50
50
50
114
138
116
118
140
120
104
106
108
110
102
Memory controller
224
3,0 pF
37,5 Ohm
VDD/2
222
210
37,5 Ohm
VDD/2
170

Fig. 5

Write to slot No:

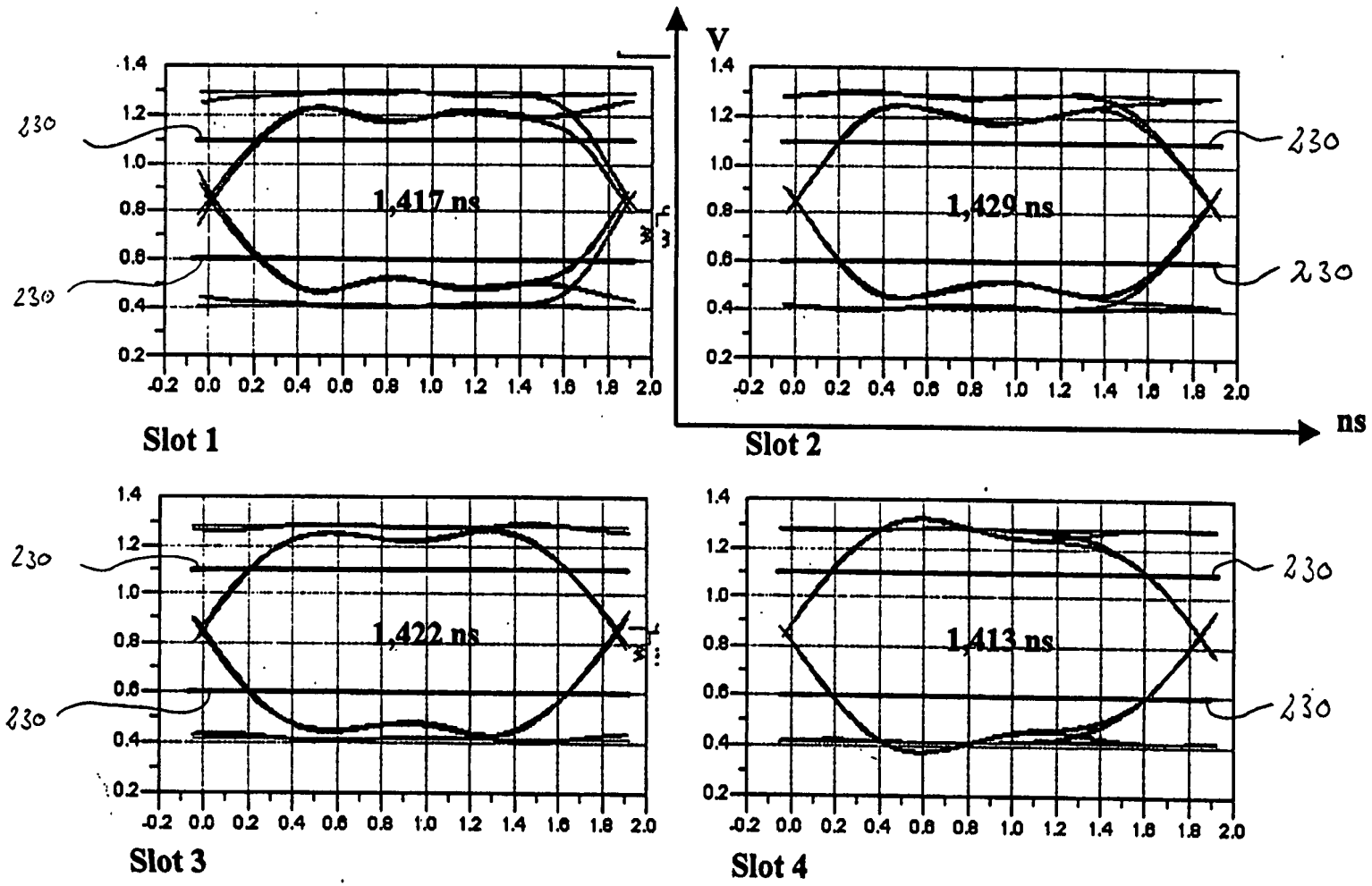

Fig. 6

Read from the slot No :

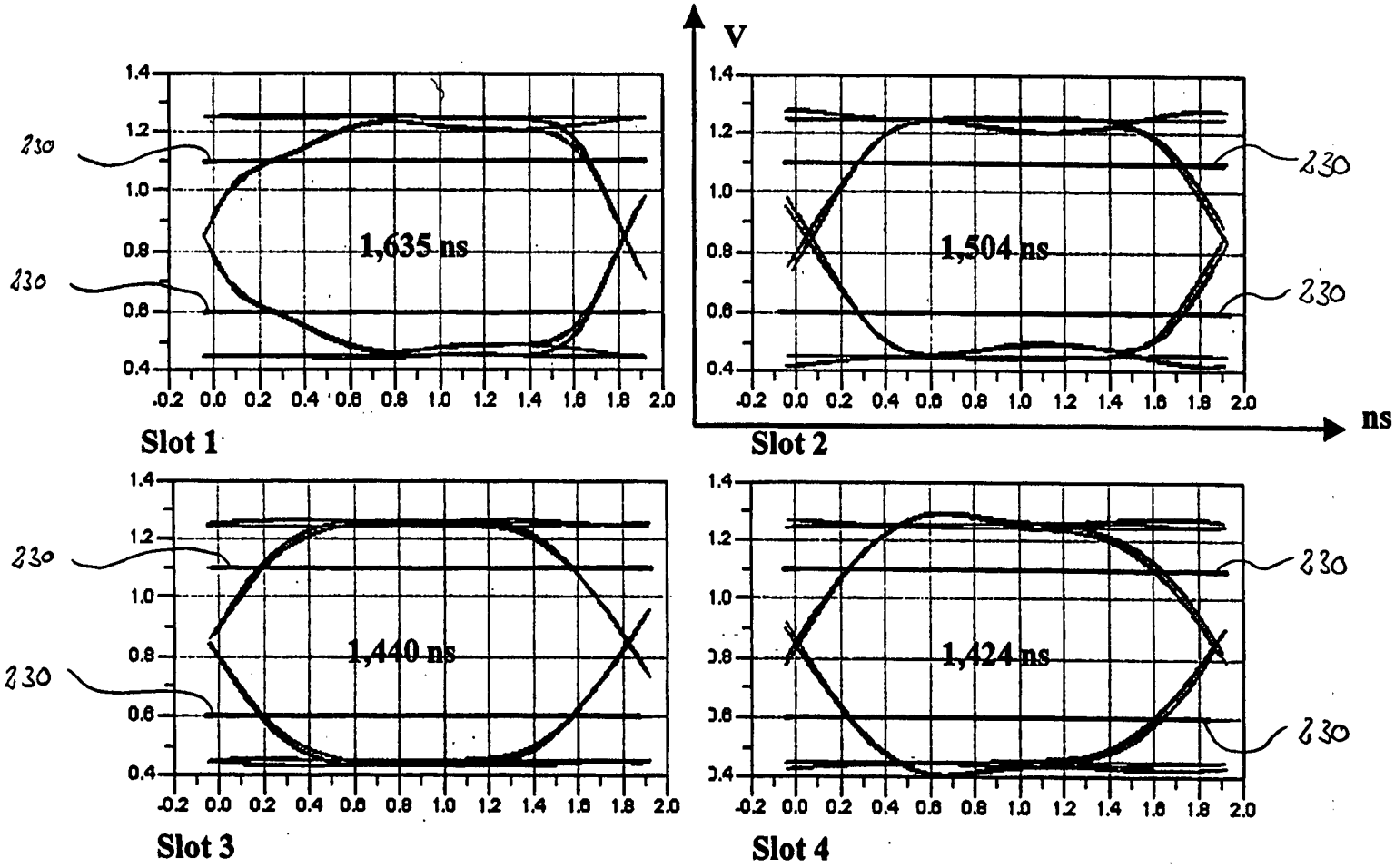

Fig. 7

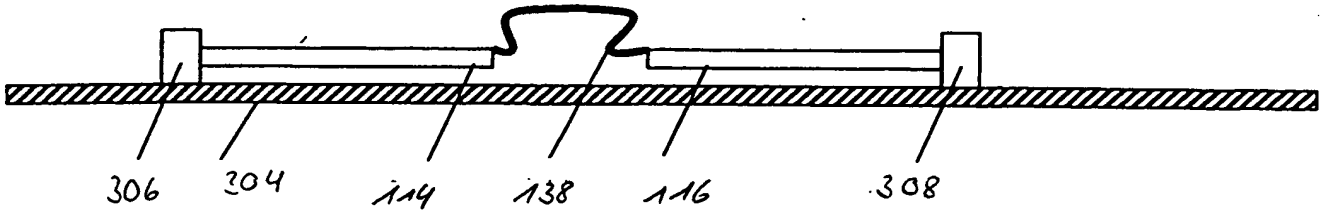

Fig. 8

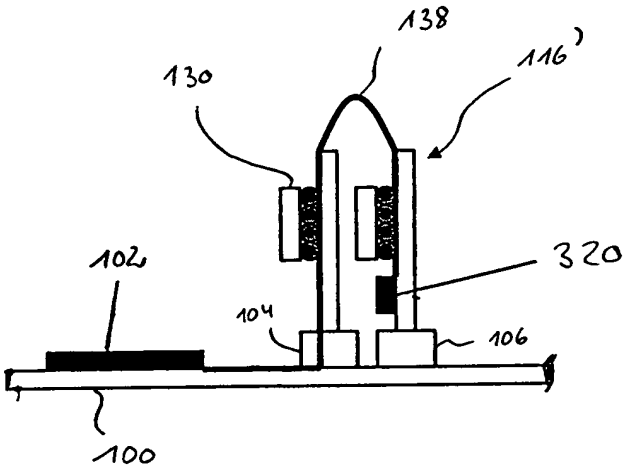

Fig. 9

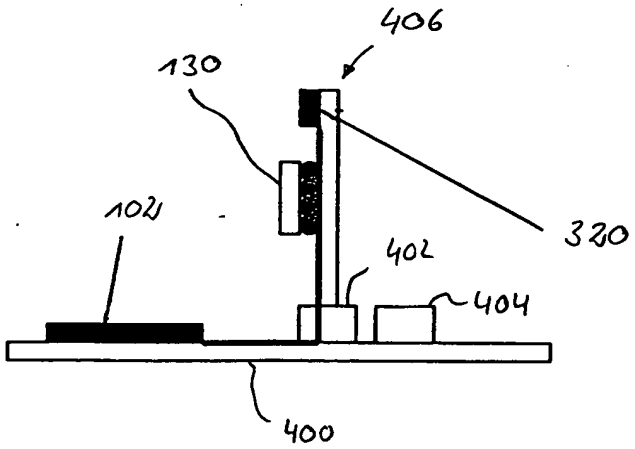

Fig. 10

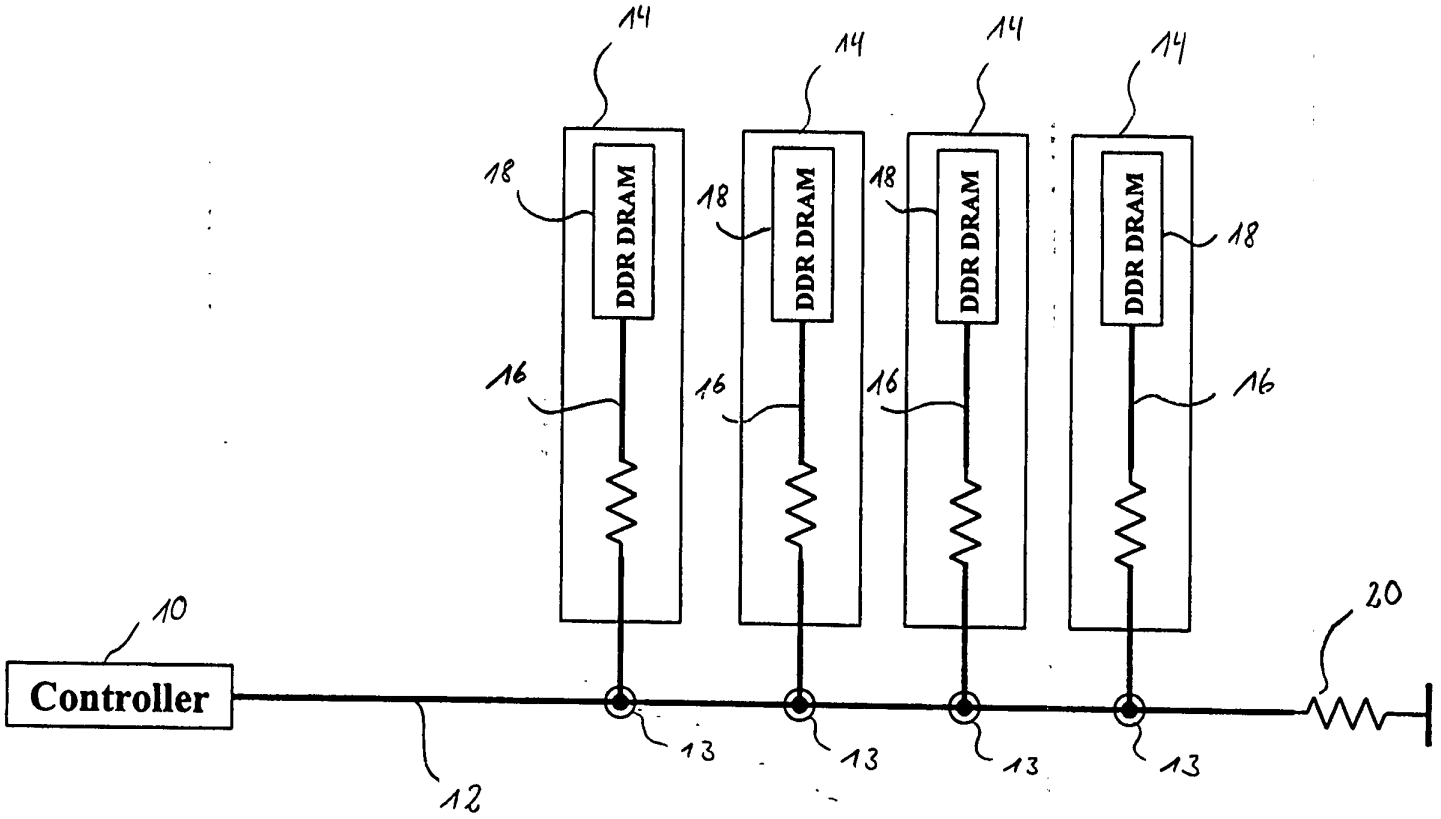

Fig. 11 (Prior Art)

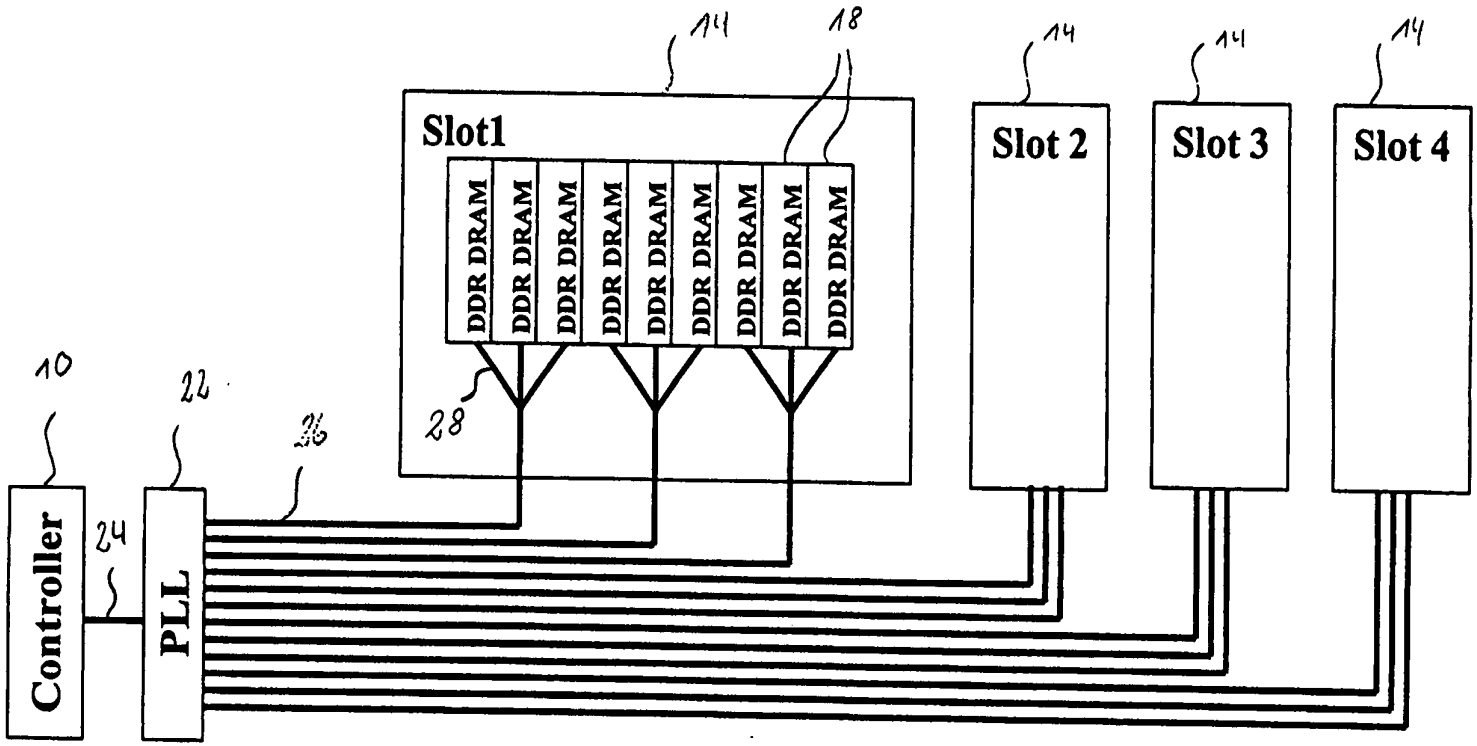

Fig. 12a (Prior Art)

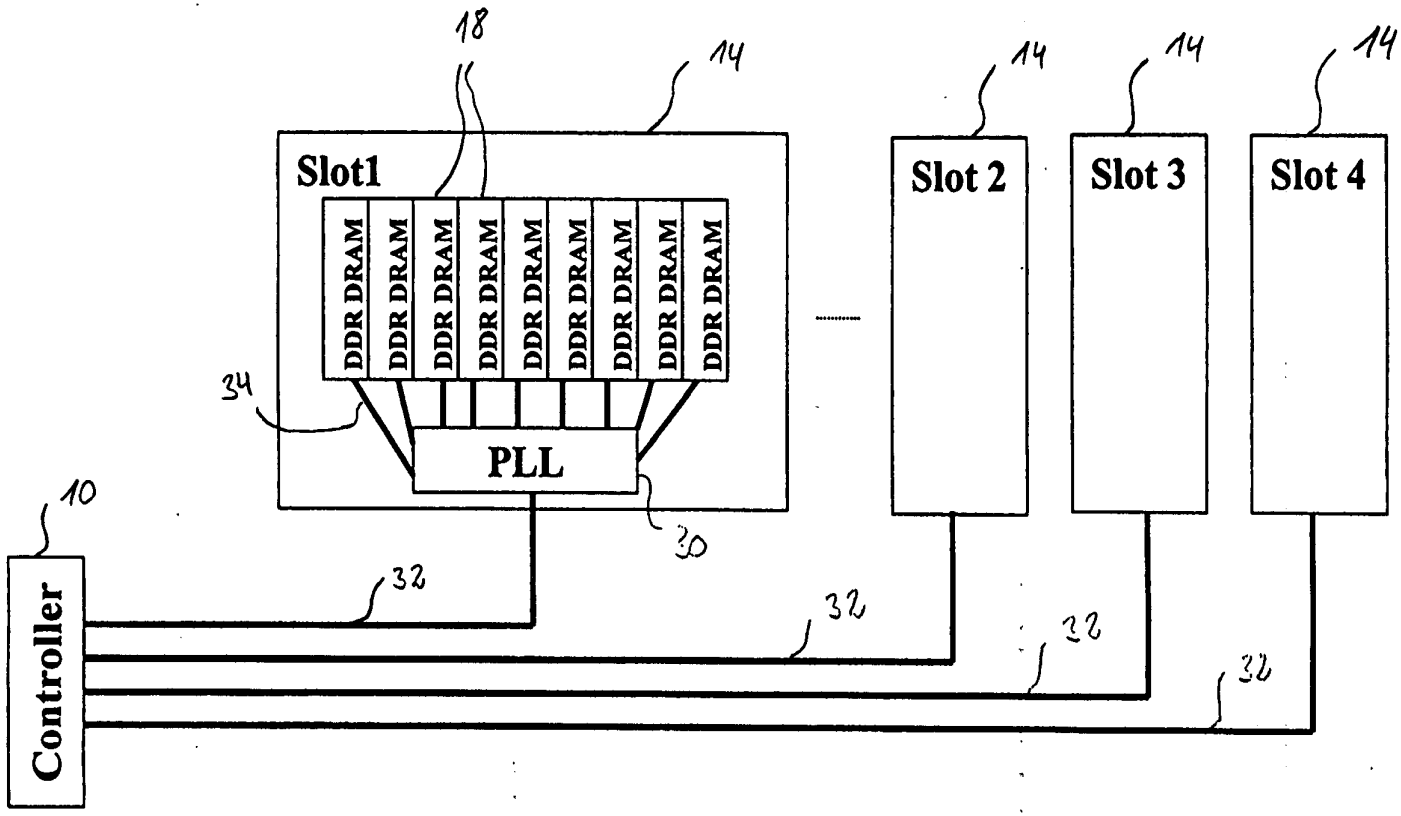

Fig. 12B (Prior Art)

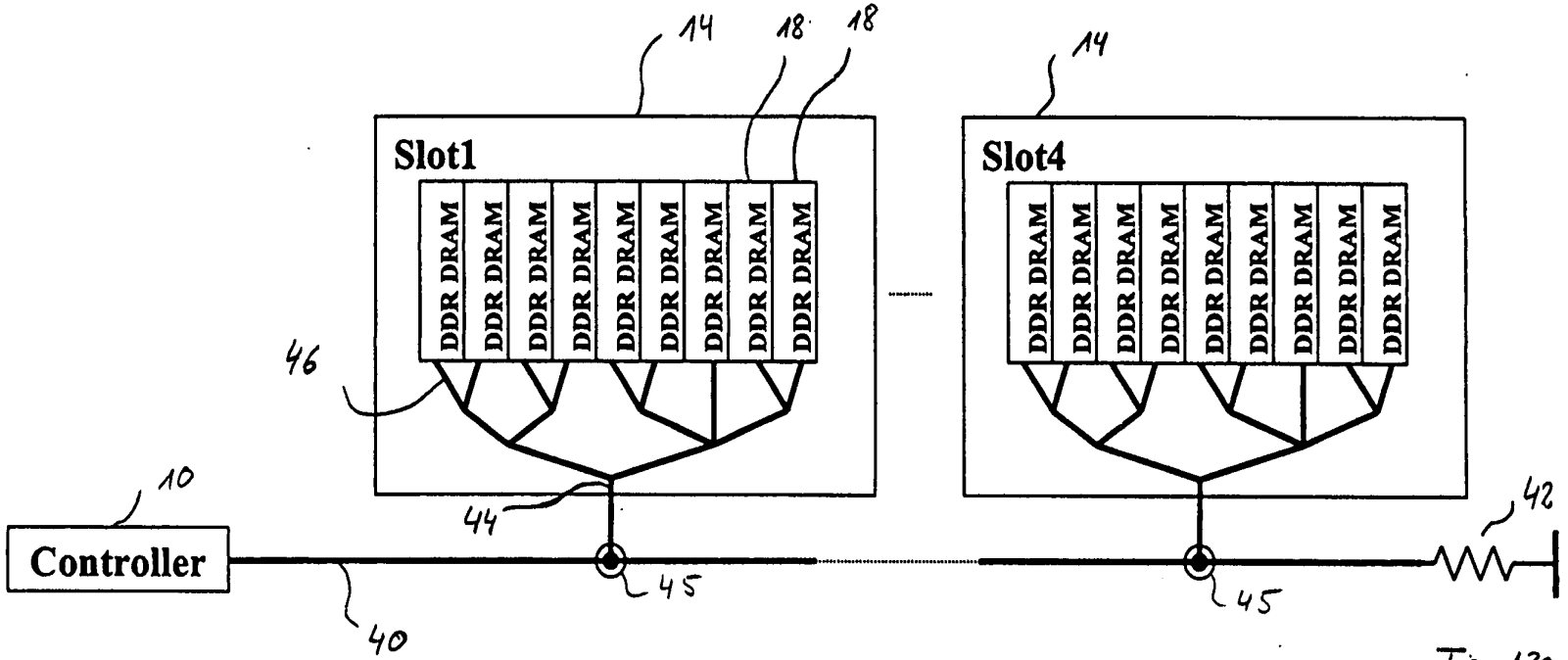

Fig. 13a (Prior Art)

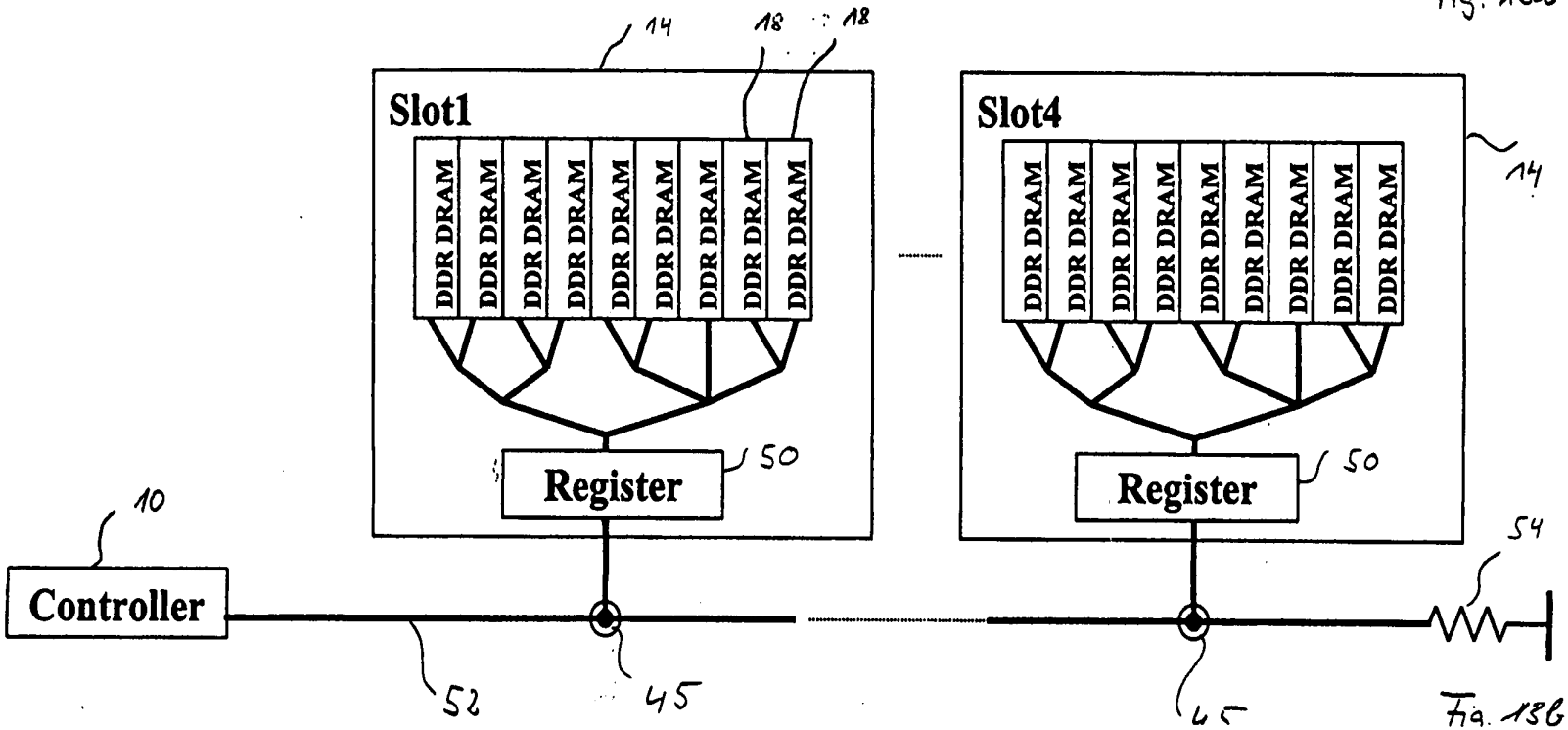

Fig. 13b (Prior Art)

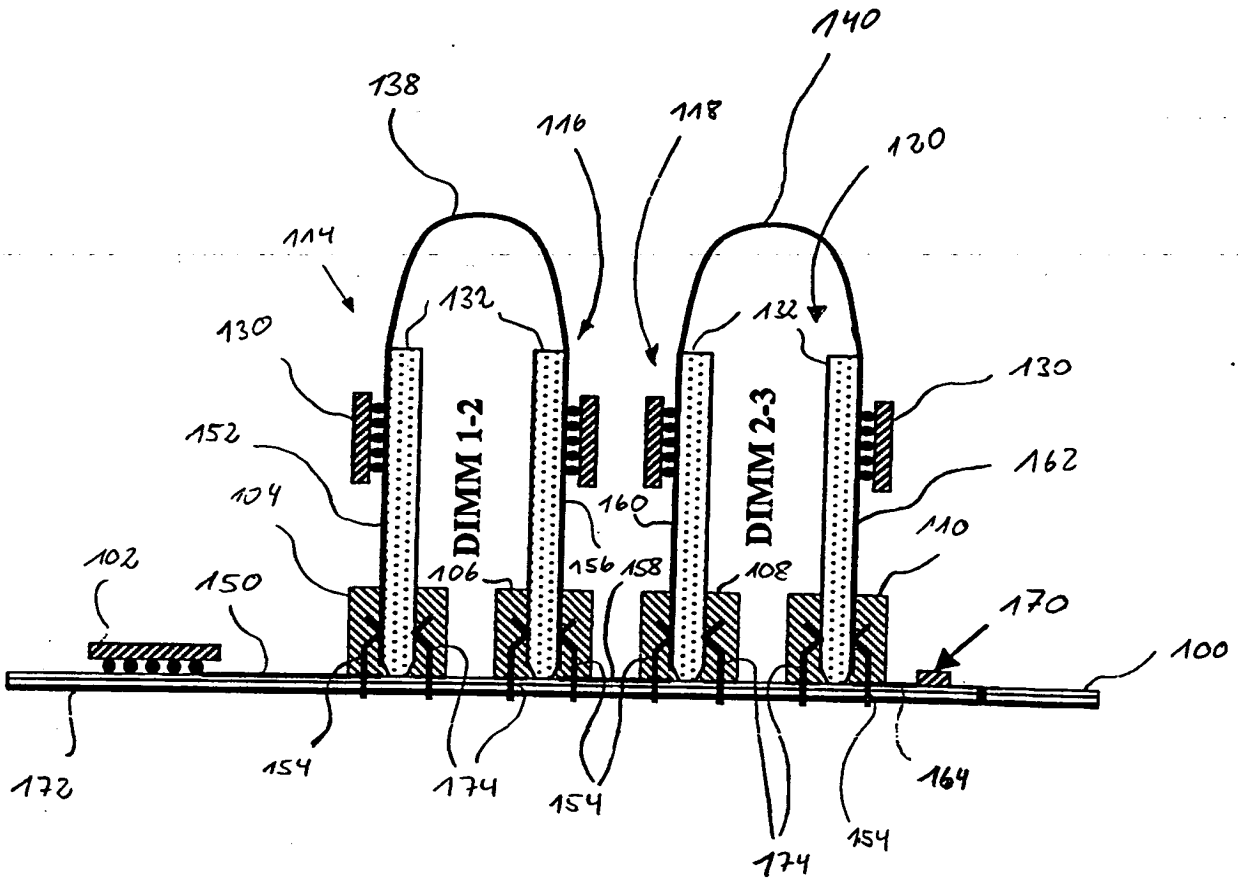

Fig. 1

Figure for abstract